

REDUCTION OF THE NUMBER OF MULTIPLICATION OPERATIONS IN DIGITAL SIGNAL PROCESSING ALGORITHMS BY CLASSICAL METHODS OF DISCRETE FOURIER TRANSFORM

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Abstract: The issues related to the problem of minimizing hardware costs in software and hardware implementation of digital algorithms of discrete Fourier transform (DFT) are considered. Possible ways of solving these problems based on the use of digital algorithms of classical methods of DFT are described. Various digital methods of direct, fast and recurrent DFT (RDFT) and number-theoretic Mersenne transforms are investigated. The purpose of the research is a comparative analysis of these methods. The research used methods of mathematical and software modeling of digital signal processing (DSP) algorithms. A comparative analysis of classical methods of DFT, which allows minimizing the required number of multiplication operations in DSP algorithms, is carried out. The results of this analysis are presented.

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The accelerated development of nanoelectronics actualizes the development of DSP algorithms by elementary nanoelectronic devices. In some cases, when constructing these algorithms, we can use the methods of DFT on digital signal processors and programmable logic devices (PLD). This stimulates the search for a solution to the problem of reducing hardware costs for software and hardware implementation of such algorithms. The urgency of the problem of reducing the number of arithmetic multiplication operations in digital DFT algorithms is determined by the growing needs for the development and improvement of DSP computational algorithms for mechanical engineering in order to reduce the amount of hardware costs for their software and hardware implementation.

This problem will be relevant, at least as long as nanoelectronics develops in the same way as microelectronics developed in its time, and the equality of the speeds of performing arithmetic operations of multiplication and addition on elementary nanoelectronic devices is achieved mainly by hardware.

The aim of the research is a comparative analysis of classical DFT methods that allow reducing the required number of multiplication operations in DSP algorithms. The research used the methods of mathematical and software modeling of digital algorithms DSP.

RDFT methods can significantly reduce the number of multiplication arithmetic operations in digital DFT algorithms designed to isolate individual spectral components of a digital signal in different parts of the frequency range and (or) different groups of spectral components of this signal. The application of RDFT methods requires recalculation of Fourier coefficients when changing their frequency resolution.

Since the further development of the idea of reducing the number of arithmetic multiplication operations in digital DFT algorithms has still not lost its significance in the hardware and software implementation of classical DFT methods, the promising development of digital algorithms for classical DFT methods should be focused on a comprehensive consideration of the reserves of reducing hardware costs required for achieving equality of the speeds of performing arithmetic operations of multiplication and addition by elementary devices of microelectronics and nanoelectronics.

The idea of reducing the number of arithmetic multiplication operations in digital DFT algorithms is due to the use of hardware to achieve equality of the speed of performing arithmetic multiplication and addition operations in elementary digital computing devices. It has been successfully implemented using FFT and DFT methods based on NTT. However, it was possible to minimize the number of arithmetic multiplication operations only in a number of digital FFT algorithms with a minimum number of arithmetic multiplication operations and DFT according to Winograd algorithm with Mersenne NTT.

Obviously, it is possible and necessary to achieve a smaller number of arithmetic multiplication operations in digital DFT algorithms by modifying the digital algorithms of FFT and (or) DFT method using Winograd algorithm with Mersenne NTT. However, in order to completely abandon arithmetic multiplication operations in digital DFT algorithms, it is necessary and sufficient to develop and improve such DFT methods that allow completely replacing arithmetic multiplication operations in digital DSP algorithms with arithmetic addition operations and (or) algorithmic shift operations.

Thank you for your attention!